

Application No.: 10/823,214

Docket No.: JCLA12708

AMENDMENT**In The Claims:**

Please amend the claims as follows:

Claim 1. (currently amended) A circuit for controlling a brushless permanent magnet motor comprising:

a plurality of windings, each of the windings having a first end connected at a common node and each of the windings having a second end connectable directly to supply voltages by switches, the second end connected to an upper supply voltage or connected to a lower supply voltage or disconnected from the supply voltages;

blocking circuitry connectable with the second ends, the blocking circuitry producing a blocked voltage, the blocked voltage representing a voltage across an associated winding;

a comparator receiving the blocked voltage on one input and a reference voltage on another input, the comparator result indicating polarity of a back emf voltage in the associated winding, wherein a non-inverting input is connected via a single direction switch to a free end of a phase at a cathode end; and

a latch providing control signals for the circuit, an input of the latch enabled by an enable signal, an output of the latch comprising a back emf voltage detection signal,

wherein the blocking circuitry and the comparator are duplicated for each of the windings.

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Claim 2. (original) The circuit of claim 1, wherein the blocking circuit further comprises:
a diode with a cathode end connected to the second end; and
a resistor with one end connected to an anode end of the diode and the other end connected to a DC power source.

Claim 3. (currently amended) A circuit for controlling a brushless permanent magnet motor comprising:

a plurality of windings, each of the windings having a first end connected at a common node and each of the windings having a second end connectable directly to supply voltages by switches, the second end connected to an upper supply voltage or connected to a lower supply voltage or disconnected from the supply voltages;

a single blocking circuitry periodically connected to the second ends for producing a blocked voltage;

a comparator receiving the blocked voltage on one input and a reference voltage on another input, the comparator result indicating polarity of a back emf voltage in the associated winding, wherein a non-inverting input is connected via a diode to a free end of a phase at a cathode end;
and

a latch providing control signals for the circuit, an input of the latch enabled by an enable signal, an output of the latch comprising a back emf voltage detection signal.

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Claim 4. (currently amended) The brushless DC motor module of claim 3, wherein the blocking circuit further comprises:

a second diode with a cathode end connected to the second end; and

a resistor with one end connected to an anode end of the second diode and the other end connected to a DC power source.

Claim 5. (currently amended) A method for controlling a brushless DC motor, wherein the brushless DC rotor comprises a rotor capable of generating a back electromotive force, the method comprising steps of:

determining whether a time of a zero crossing point for the back electromotive force is detected;

determining a rotor speed of the brushless DC motor is smaller than a lower speed if the time of the zero crossing point is detected;

reducing a frequency of a control signal if the rotor speed is smaller than the lower speed;

determining again whether there is a time of a zero crossing point; ~~and~~

terminating the method upon not detecting the zero crossing point; and

resetting the frequency of the control signal if the time of the zero crossing point is detected again.

Claim 6. (original) The method of claim 5, further comprising step of determining again whether a time of a zero crossing point when the rotor speed is larger than the lower speed.

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Claim 7. (canceled)

Claim 8. (original) The method of claim 5, wherein the control signal is a pulse width modulation (PWM) signal.

Claim 9. (original) The method of claim 5, wherein in step of resetting the frequency, the frequency is reset to a normal operation frequency.